IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 49 and 73 and CANCEL claim 56, without prejudice or disclaimer, in accordance with the following:

49. (CURRENTLY AMENDED) A branch history information write control device in an instruction execution processing apparatus, comprising:

a memory unit storing an instruction string;

branch prediction unit performing a branch prediction of a branch instruction; and

a control unit controlling the memory unit and the branch prediction unit in such a way that writing of branch history information in the branch prediction unit and control over fetching of the instruction string in the memory unit may not occur simultaneously,

wherein ~~a fetch request of the instruction string precedes writing of the branch history information~~said control unit uses a counter to count several clock cycles (several states) to delay, for a period of several clock cycles (several states), the writing of the branch history information and control, beforehand, the fetching of the instruction string.

50. (PREVIOUSLY PRESENTED) The device according to claim 49, wherein said control unit writes the branch history information in said branch prediction unit in a timing such that said memory unit cannot accept an instruction fetch request.

51. (PREVIOUSLY PRESENTED) The device according to claim 49, wherein said control unit writes the branch history information in said branch prediction unit in a timing for making an instruction pre-fetch request.

52. (PREVIOUSLY PRESENTED) The device according to claim 49, wherein when writing in said branch prediction unit the branch history information about a branch instruction which has failed in a branch prediction, said control unit writes the branch history information in

said branch prediction unit after several clock cycles (several states).

53. (PREVIOUSLY PRESENTED) The device according to claim 49, wherein when writing in said branch prediction unit the branch history information about a branch instruction which has failed in a branch prediction, said control unit writes the branch history information in said branch prediction unit after a re-instruction fetch request by the branch instruction is executed and several clock cycles (several states) after the re-instruction fetch request is executed.

54. (PREVIOUSLY PRESENTED) The device according to claim 49, wherein if the instruction execution processing apparatus is provided with a temporary instruction buffer unit temporarily storing an instruction string outputted from said memory unit,

said control unit writes the branch history information of the branch instruction in said branch prediction unit several clock cycles (several states) after there is a write request of a branch instruction if the temporary instruction buffer unit is empty and there is no instruction fetch request.

55. (PREVIOUSLY PRESENTED) The device according to claim 49, wherein if the instruction execution processing apparatus is provided with a temporary instruction buffer unit temporarily storing an instruction string outputted from said memory unit,

said control unit does not promptly write a branch history of a branch instruction to be requested to be written in said branch prediction unit, waits for a next instruction fetch request and writes the branch history information of the branch instruction several clock cycles (several states) after the instruction fetch request is executed if the temporary instruction buffer unit is empty and there is not even one instruction fetch request.

56. (CANCELLED) A branch history information write control device in an instruction execution processing apparatus, comprising:

a memory unit storing an instruction string;

branch prediction unit performing a branch prediction of a branch instruction; and

a control unit controlling the memory unit and the branch prediction unit in such a way that writing of branch history information in the branch prediction unit and control over fetching of the instruction string in the memory unit may not occur simultaneously,

wherein said control unit uses a counter to count several clock cycles (several states).

57. (PREVIOUSLY PRESENTED) The device according to claim 49, wherein when writing the branch history information of the branch instruction which has failed in the branch prediction, said control unit writes the branch history information after an instruction decoding unit or said temporary instruction buffer unit in the instruction execution processing apparatus receives a fetch instruction string corresponding to a re-instruction fetch requested by the branch instruction.

58. (PREVIOUSLY PRESENTED) The device according to claim 49, further comprising:

a write reservation station unit temporarily storing the branch history information to be written.

59. (PREVIOUSLY PRESENTED) The device according to claim 58, wherein said control unit registers in the reservation station unit only the branch history information concerning a branch instruction which must be written in said branch prediction unit.

60. (PREVIOUSLY PRESENTED) The device according to claim 59, wherein the branch history information is about at least one of a new entry registration, an entry content change or an entry erasure.

61. (PREVIOUSLY PRESENTED) The device according to claim 58, wherein if said write reservation station unit is full and there is a request for registering in the write reservation station unit, said control unit writes in said branch prediction unit least one group of branch history information, writing of which in the write reservation station unit is held and the branch history information of which has been requested to be registered.

62. (PREVIOUSLY PRESENTED) A branch history information write control device in an instruction execution processing apparatus, comprising:

a memory unit storing an instruction string;

branch prediction unit performing a branch prediction of a branch instruction;

a control unit controlling the memory unit and the branch prediction unit in such a way

that writing of branch history information in the branch prediction unit and control over fetching of the instruction string in the memory unit may not occur simultaneously; and

a write reservation station unit temporarily storing the branch history information to be written,

wherein if said branch prediction unit is configured to simultaneously write a plurality of entries and said write reservation station unit stores a plurality of valid information, writing of which is held, said control unit simultaneously writes the plurality of information in a timing such that writing in said branch prediction unit is possible.

63. (PREVIOUSLY PRESENTED) The device according to claim 49, wherein if an instruction is conditionally encoded or branched by an execution completion of an execution instruction, which exits before a branch instruction, there is another branch instruction before the branch instruction when a branch destination address is confirmed, and even if the branch instruction cannot be completed, said control unit writes the branch history information of the branch instruction in said branch prediction unit or registers the information in the write reservation station unit.

64. (PREVIOUSLY PRESENTED) A branch history information write control device in an instruction execution processing apparatus, comprising:

a memory unit storing an instruction string;

branch prediction unit performing a branch prediction of a branch instruction; and

a control unit controlling the memory unit and the branch prediction unit in such a way that writing of branch history information in the branch prediction unit and control over fetching of the instruction string in the memory unit may not occur simultaneously,

wherein if an instruction is conditionally encoded or branched by an execution completion of an execution instruction, which exits before a branch instruction, there is another branch instruction before the branch instruction when a branch destination address is confirmed, and even if the branch instruction cannot be completed, said control unit writes the branch history information of the branch instruction in said branch prediction unit or registers the information in the write reservation station unit,

wherein said control unit provides a flag indicating that the branch history information is written or registered in the write reservation station unit for each corresponding branch instruction being processed.

65. (PREVIOUSLY PRESENTED) The device according to claim 58, wherein said control unit writes the branch history information, writing of which in the write reservation station unit is held when an execution of an instruction is completed.

66. (PREVIOUSLY PRESENTED) The device according to claim 58, wherein said control unit writes branch history information of a corresponding entry in said branch prediction unit or said write reservation station unit when an execution of an instruction is completed.

67. (PREVIOUSLY PRESENTED) The device according to claim 58, wherein if the instruction execution processing apparatus is provided with a unit controlling an execution completion of an instruction in its instruction control unit,

said control unit stores an ID assigned for each instruction, which is stored in the execution completion management unit, in an entry of the write reservation station unit.

68. (PREVIOUSLY PRESENTED) The device according to claim 58, wherein if it is confirmed that a branch instruction corresponding to a valid entry of the write reservation station unit is neither executed nor completed due to an occurrence of interruption, the entry corresponding to the write reservation station unit is nullified.

69. (PREVIOUSLY PRESENTED) The device according to claim 49, further comprising:

a bypass unit making branch history information, writing of which in said branch prediction unit is held, a research target of a branch prediction.

70. (PREVIOUSLY PRESENTED) The device according to claim 58, further comprising:

a bypass unit making the branch history information of the branch instruction a research target of a branch prediction, wherein the branch instruction comprises the write reservation station unit.

71. (PREVIOUSLY PRESENTED) The device according to claim 70, wherein said bypass unit makes the branch history information a search target of a branch prediction when a

conditional code for the branch instruction is confirmed if it is confirmed that the branch instruction is not branched and when a branch destination address is confirmed if it is confirmed that the branch instruction is branched.

72. (PREVIOUSLY PRESENTED) The device according to claim 49, wherein a dual-port RAM in which writing and reading can be simultaneously executed independently is used for said branch prediction unit to hold an entry.

73. (CURRENTLY AMENDED) An instruction control method in an apparatus provided with both a memory storing an instruction string, and a branch prediction unit performing a branch prediction of a branch instruction, comprising:

controlling the memory unit and the branch prediction unit in such a way that writing of branch history information in said branch prediction unit and control over fetching of the instruction string in the memory do not occur simultaneously; and

counting several clock cycles (several states) to delay, for a period of several clock cycles (several states), the writing of the branch history information and control, beforehand, the fetching of the instruction string,

~~wherein a fetch request of the instruction string precedes writing of the branch history information~~.

74. (PREVIOUSLY PRESENTED) The method according to claim 73, wherein the branch history information is written in said branch prediction unit in a timing such that said memory cannot accept an instruction fetch request.

75. (PREVIOUSLY PRESENTED) The method according to claim 73, wherein the branch history information is written in said branch prediction unit in a timing of requesting a pre-fetch of an instruction.

76. (PREVIOUSLY PRESENTED) The method according to claim 73, wherein if the branch history information of a branch instruction which has failed in a branch prediction is written in said branch prediction unit, the branch history information is written in said branch prediction unit after several clock cycles (several states).

77. (PREVIOUSLY PRESENTED) The method according to claim 73, wherein if the branch history information of a branch instruction which has failed in a branch prediction is written in said branch prediction unit, the branch history information is written in said branch prediction unit after a re-instruction fetch request by the branch instruction is executed and several clock cycles (several states) after the re-instruction fetch request is executed.

78. (PREVIOUSLY PRESENTED) The method according to claim 73, further comprising:

temporary instruction buffer operation temporarily storing an instruction string, outputted by said memory,

wherein if there is no instruction string to be stored in the temporary instruction buffer operation and there is no instruction fetch request, the branch history information of a branch instruction to be requested to be written is written in said branch prediction unit several clock cycles (several states) after a write request is issued.

79. (PREVIOUSLY PRESENTED) The method according to claim 73, further comprising:

temporary instruction buffer operation temporarily storing an instruction string, outputted by said memory,

wherein if there is no instruction string to be stored in the temporary instruction buffer operation and there is no instruction fetch request, the branch history information of a branch instruction to be requested to be written is not promptly written in said branch prediction unit, waits for a next instruction fetch request and is written several clock cycles (several states) after the instruction fetch request is executed.

80. (PREVIOUSLY PRESENTED) The method according to claim 73, wherein when the branch history information of a branch instruction which has failed in a branch prediction is written in said branch prediction unit, the branch history information is written after its instruction decoding unit or said temporary instruction buffer receives a fetch instruction string corresponding to a re-instruction fetch requested by the branch instruction.

81. (PREVIOUSLY PRESENTED) The method according to claim 73, further comprising:

write reservation station operation temporarily storing the branch history information to be written.

82. (PREVIOUSLY PRESENTED) The method according to claim 81, wherein only the branch history information concerning a branch instruction which must be written in said branch prediction unit is registered in said write reservation station operation.

83. (PREVIOUSLY PRESENTED) The method according to claim 82, wherein the branch history information is a new entry registration, an entry content change or an entry erasure.

84. (PREVIOUSLY PRESENTED) The method according to claim 81, wherein if a storage capacity in the write reservation station operation is full and further there is a register request on a branch instruction, branch history information of which must be written in the write reservation station operation, at least one group of a branch history information, writing of which is held in the write reservation station operation and the branch history information which has been requested to be registered, is written.

85. (PREVIOUSLY PRESENTED) An instruction control method in an apparatus provided with both a memory storing an instruction string, and a branch prediction unit performing a branch prediction of a branch instruction, comprising:

controlling the memory unit and the branch prediction unit in such a way that writing of branch history information in said branch prediction unit and control over fetching of the instruction string in the memory do not occur simultaneously; and

a write reservation station operation temporarily storing the branch history information to be written,

wherein if said branch prediction unit is configured to simultaneously write a plurality of entries and the write reservation station unit stores a plurality of valid information, writing of which is held, a plurality of writing executions are performed in a timing such that writing in said branch prediction unit is available.

86. (PREVIOUSLY PRESENTED) The method according to claim 73, wherein if an instruction is conditionally encoded or branched by an execution completion of an execution

instruction, which exists before a branch instruction, there is another branch instruction before the branch instruction when a branch destination address is confirmed and even if the branch instruction cannot be completed, the branch history information of the branch instruction is written in said branch prediction unit or registered in the reservation station operation.

87. (PREVIOUSLY PRESENTED) An instruction control method in an apparatus provided with both a memory storing an instruction string, and a branch prediction unit performing a branch prediction of a branch instruction, comprising:

controlling the memory unit and the branch prediction unit in such a way that writing of branch history information in said branch prediction unit and control over fetching of the instruction string in the memory do not occur simultaneously,

wherein if an instruction is conditionally encoded or branched by an execution completion of an execution instruction, which exists before a branch instruction, there is another branch instruction before the branch instruction when a branch destination address is confirmed and even if the branch instruction cannot be completed, the branch history information of the branch instruction is written in said branch prediction unit or registered in the reservation station operation,

wherein a flag indicating that the branch history information is written or registered in said write reservation station operation is provided for each corresponding branch instruction being processed.

88. (PREVIOUSLY PRESENTED) The method according to claim 81, wherein branch history information, writing of which is held in said write reservation station operation, is written when an execution of an instruction is completed.

89. (PREVIOUSLY PRESENTED) The method according to claim 81, wherein branch history information of a corresponding entry is written in said write reservation station unit when execution of an instruction is completed.

90. (PREVIOUSLY PRESENTED) The method according to claim 81, wherein an instruction control unit further comprises the operation of managing an execution completion of an instruction, and stores an ID assigned for each instruction which is stored in said execution completion management operation, in an entry in said write reservation station operation.

91. (PREVIOUSLY PRESENTED) The method according to claim 81, wherein if it is found that a branch instruction corresponding to a valid entry stored in said write reservation station operation due to an occurrence of interruption, is not executed and completed, a corresponding entry stored in said write reservation station operation is nullified.

92. (PREVIOUSLY PRESENTED) The method according to claim 73, wherein branch history information, writing of which in said branch prediction unit is held, is a search target of a branch prediction.

93. (PREVIOUSLY PRESENTED) The method according to claim 81, wherein branch history information of a branch instruction which is being' executed in said write reservation station operation, is a search target of a branch prediction.

94. (PREVIOUSLY PRESENTED) The method according to claim 93, wherein the branch history information is a search target of a branch prediction when a conditional code for the branch instruction is confirmed if it is confirmed that the branch instruction is not branched, and when a branch destination address is confirmed if it is confirmed that the branch instruction is branched.